Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (original) A peripheral device having a bus-controlled switching arrangement for operating a power supply, the device comprising:

a bus interface adapted for communicating with a remote device via a bus; and

a switch circuit connected between the bus interface and a power supply, the switch circuit operative, when the power supply is in an inactive state, for sensing bus activity and providing a voltage signal for activating the power supply in response to said sensed bus activity, and wherein the switch circuit has no power dissipation when no activity is present on the bus.

2. (original) The device of claim 1, wherein the switch circuit comprises a first switching transistor having an input coupled to said bus interface, wherein the first switching transistor is brought from a non-conducting state to a conducting state in the presence of pulse signals at said input.

3. (original) The device of claim 2, wherein the switch circuit further comprises a second switching transistor having an input coupled to a capacitor, wherein the second switching transistor is brought from a non-conducting state to a conducting state in response to a charge on said capacitor exceeding a threshold level when said first switching transistor is in said conducting state.

4. (original) The device of claim 3, wherein the switch circuit further comprises a capacitor coupled to the output of the second switching transistor for providing an input voltage to a control circuit of the power supply for activating or inactivating the power supply according to the level of the input voltage.

4. (original) The device of claim 1, wherein the power supply further includes a latching circuit responsive to initial activation of said power supply for providing a voltage signal to the power supply sufficient to maintain the power supply in an active state independent of the bus activity.

5. (original) The device of claim 4, further comprising a control input coupled to said power supply for receiving a control signal to cause said power supply to become inactive.

6. (original) The device of claim 1, further comprising means for bypassing said switch circuit to provide a path from a source of input supply voltage to said power supply to cause activation of the power supply independent of bus activity.

7. (original) The device of claim 1, wherein the power supply is inactivated after a given time delay based on an absence of bus activity.

8. (original) A peripheral device having a bus-controlled switching arrangement for operating a power supply, the device comprising:

a bus interface adapted for communicating with a remote device via a bus;

first and second switching transistors;

first and second capacitors, said first capacitor coupled to said first switching transistor, said second capacitor coupled between said second switching transistor and a power supply; wherein said first switching transistor is coupled to said bus interface and dissipates no power when no pulses are present on said bus interface, and wherein, in response to the presence of pulses on said bus interface, said first switching transistor is activated to charge said first capacitor to activate said second switching transistor for generating a voltage signal at said second capacitor sufficient to activate said power supply.

9. (original) The device of claim 8, wherein said power supply further includes a control input for receiving a control signal in response to inactivity on said bus interface over a predetermined interval, and inactivating the power supply in response thereto.

10. (original) The device of claim 8, further comprising a resistor coupled to a source of input voltage and to said second switching transistor for, when said second transistor is conducting, charging said second capacitor to a voltage sufficient to activate said power supply.

11. (original) The device of claim 8, wherein the power supply is inactivated after a given time delay based on an absence of bus activity.

12. (original) The device of claim 11, wherein the time delay includes a delay associated with the discharging of said first and second capacitors in said switching circuit when no bus activity is sensed.

13. (original) The device of claim 8, wherein the bus comprises an ethernet bus and said bus activity comprises a sequence of scanning pulses.

14. (original) A perhipheral device responsive to an input data signal developed on a bus, comprising:

a power supply controller for controlling a power supply for the peripheral device; and

a transistor having a first main current conducting terminal coupled to a source of an input supply voltage, a second main current conducing terminal coupled to an input supply terminal of said controller and a control terminal responsive to said data signal applied to said control terminal and having a magnitude that exceeds a threshold voltage of said transistor, when said data signal is indicative of bus activity for energizing said controller when said threshold voltage is exceeded, said transistor remaining in a passive, non-conductive state without dissipating power when said data signal is absent that is indicative of bus inactivity, for maintaining said controller de-energized.

15. (original) The peripheral device according to claim 14 wherein said second main current conducting terminal is coupled to a filter capacitor for providing noise immunity.

16. (original) The peripheral device according to claim 14 wherein said threshold voltage is determined by an emitter-base junction of said transistor.